**Experiment 8**

**Introduction to Verilog HDL Programming for designing digital Circuitry**

**Objective**

In this lab students will

* Understand the syntax of Verilog HDL for writing programs.

**Introduction to Verilog HDL**

Manual methods for designing logic circuits are feasible only when the circuit is small. For anything else (i.e., a practical circuit), designers use computer-based design tools. Coupled with the correct-by-construction methodology, computer-based design tools leverage the creativity and the effort of a designer and reduce the risk of producing a flawed design. Prototype integrated circuits are too expensive and time consuming to build, so all modern design tools rely on a hardware description language to describe, design, and test a circuit in software before it is ever manufactured.

**A *hardware description language* (HDL)** is a computer-based language that describes the hardware of digital systems in a textual form. It resembles an ordinary computer programming language, such as C, but is specifically oriented to describing hardware structures and the behavior of logic circuits. It can be used to represent logic diagrams, truth tables, Boolean expressions, and complex abstractions of the behavior of a digital system. One way to view an HDL is to observe that it describes a relationship between signals that are the inputs to a circuit and the signals that are the outputs of the circuit. For example, an HDL description of an AND gate describes how the logic value of the gate’s output is determined by the logic values of its inputs.

**Module Declaration**

The language reference manual for the Verilog HDL presents a syntax that describes precisely the constructs that can be used in the language. In particular, a Verilog model is composed of text using keywords, of which there are about 100. Keywords are predefined lowercase identifiers that define the language constructs. Examples of keywords are **module**, **endmodule**, **input**, **output**, **wire**, **and**, **or**, and **not**. For clarity, keywords will be displayed in boldface in the text in all examples of code and wherever it is appropriate to call attention to their use. Any text between two forward slashes ( *//* ) and the end of the line is interpreted as a comment and will have no effect

on a simulation using the model. Multiline comments begin with / \* and terminate with \* /. Blank spaces are ignored, but they may not appear within the text of a keyword, a user-specified identifier, an operator, or the representation of a number. **Verilog is case sensitive, which means that uppercase and lowercase letters are distinguishable (e.g., not is not the same as NOT).** The term *module* refers to the textenclosed by the keyword pair **module** . . . **endmodule**. A module is the fundamentaldescriptive unit in the Verilog language. It is declared by the keyword **module** andmust always be terminated by the keyword **endmodule**.

**Boolean Expressions**

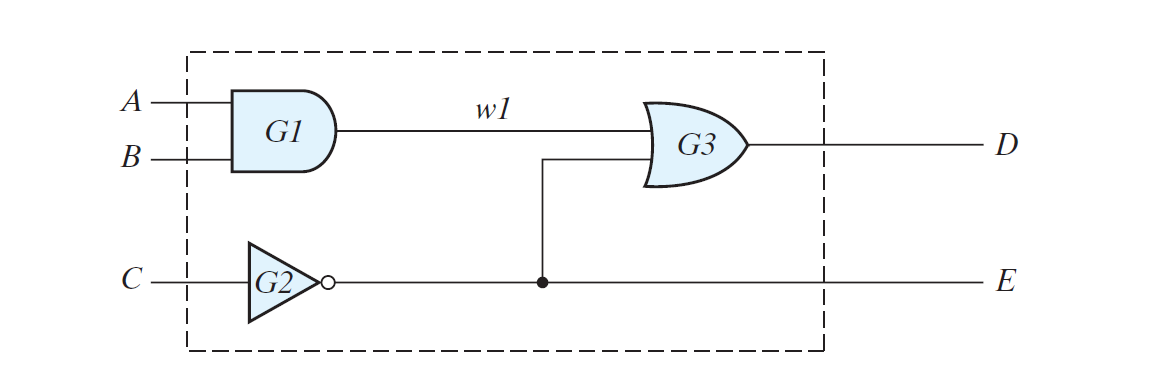
Boolean equations describing combinational logic are specified in Verilog with a continuous assignment statement consisting of the keyword **assign** followed by a Boolean expression. To distinguish arithmetic operators from logical operators, Verilog uses the symbols (&), (/), and (&) for AND, OR, and NOT (complement), respectively.

**Note: please visit the following links for understanding how to install and create your first program in Xilinx ISE Suite**

[**https://www.youtube.com/watch?v=VMEIPCjqinA&t=50s**](https://www.youtube.com/watch?v=VMEIPCjqinA&t=50s)

[**https://www.youtube.com/watch?v=5GxOKfoDqy0**](https://www.youtube.com/watch?v=5GxOKfoDqy0)

**Consider the following circuit diagram.**



**The Verilog code for circuit is:**

**module** Simple\_Circuit (A, B, C, D, E);

**output** D, E;

**input** A, B, C;

**wire** w1;

**and** G1 (w1, A, B); // Optional gate instance name

**not** G2 (E, C);

**or** G3 (D, w1, E);

**endmodule**

**Task 1:**

**run the above code and show the test bench waveforms for it. [2]**

**Task 2:**

**Now, consider the Boolean expression given below. Write down the Verilog module for it. [2]**

*E* = *A* + *BC* + *B*\_*D*

*F* = *B*’*C* + *BC*’*D*’

The equations specify how the logic values *E* and *F* are determined by the values of *A, B, C,* and *D*.

//Verilog model: Circuit with Boolean expressions

**module** Circuit\_Boolean\_CA (E, F, A, B, C, D);

**output** E, F;

**input** A, B, C, D;

**assign** E =A || (B && C) || ((!B) && D);

**assign** F =((!B) && C) || (B && (!C) && (!D));

**endmodule**

**run the above code and show the test bench waveforms for it.**

**Lab Exercise**

Find the syntax errors in the following declarations (note that names for primitive gates are optional): [2]

**module** Exmpl-3(A, B, C, D, F) // Line 1

**inputs** A, B, C, Output D, F, // Line 2

**output** B // Line 3

**and** g1(A, B, D); // Line 4

**not** (D, A, C), // Line 5

**OR** (F, B; C); // Line 6

**endmodule;** // Line 7

Draw the logic diagram of the digital circuit specified by the following Verilog description: [3]

(a) **module** Circuit\_A (A, B, C, D, F);

**input** A, B, C, D;

**output** F;

**wire** w, x, y, z, a, d;

**or** (x, B, C, d);

**and** (y, a ,C);

**and** (w, z ,B);

and (z, y, A);

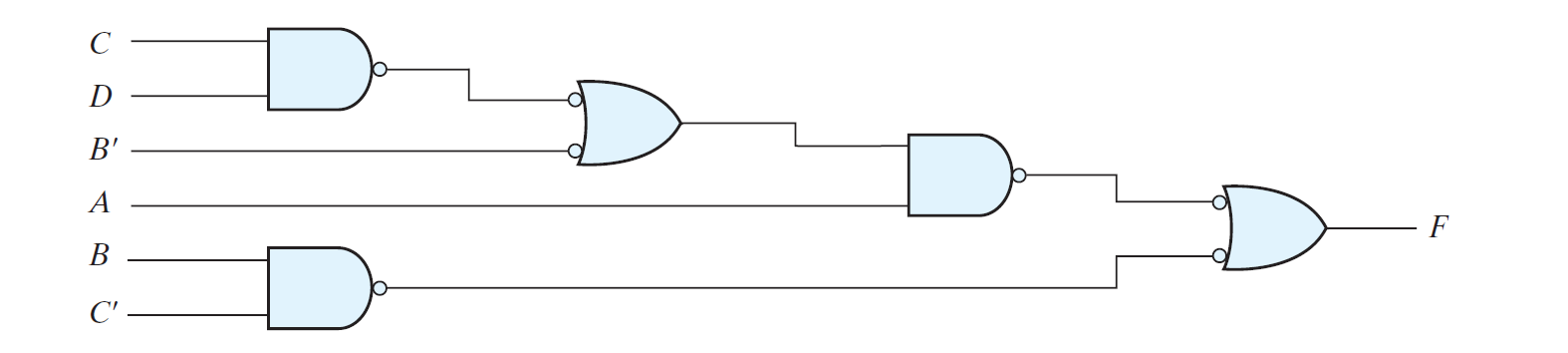
**or** (F, x, w);

**not** (a, A);

**not** (d, D);

**endmodule**

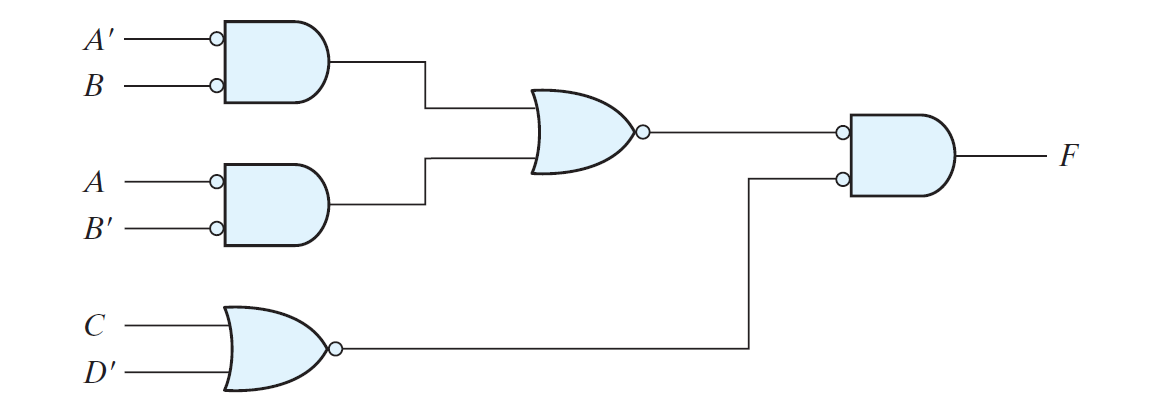
Write a Verilog gate-level description of the circuit shown in figure below. Also show test bench waveforms for it. [5+5]



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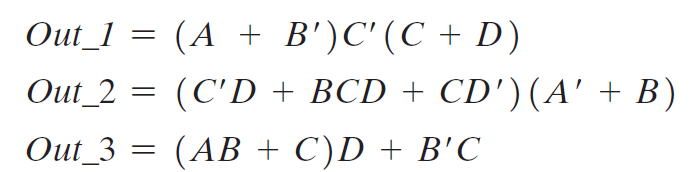


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Using continuous assignments, write a Verilog description of the circuit specified by the following Boolean functions:



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