**Experiment No. 9**

**To study the operation of S-R Latch and D latch**

**Objective**

In this lab students will

* Design an S-R latch and a D latch using NAND and NOR gates.

**Components**

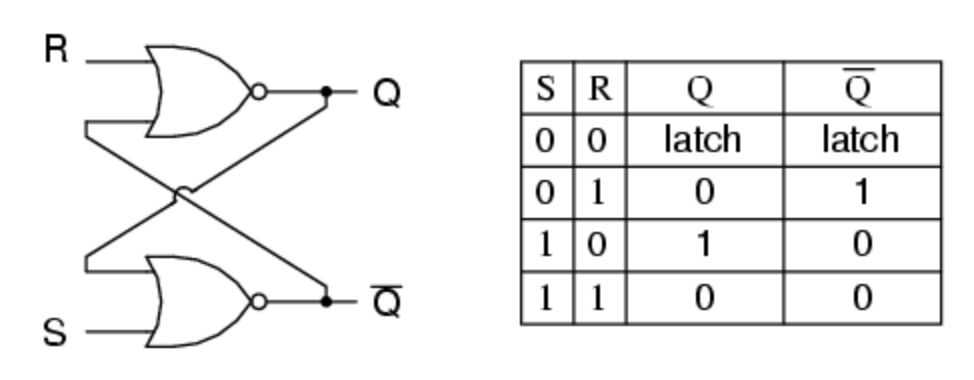
* IC74LS00×1
* IC74LS02×1
* AM2000 TRAINER
* Multimeter
* Cutter
* Single core wire
* Pair of Pliers

**Theory**

**S-R (Set-Reset) Latch:**

A bistable multivibrator has *two* stable states, as indicated by the prefix *bi* in its name. Typically, one state is referred to as *set* and the other as *reset*. The simplest bistable device, therefore, is known as a *set-reset*, or S-R, latch.

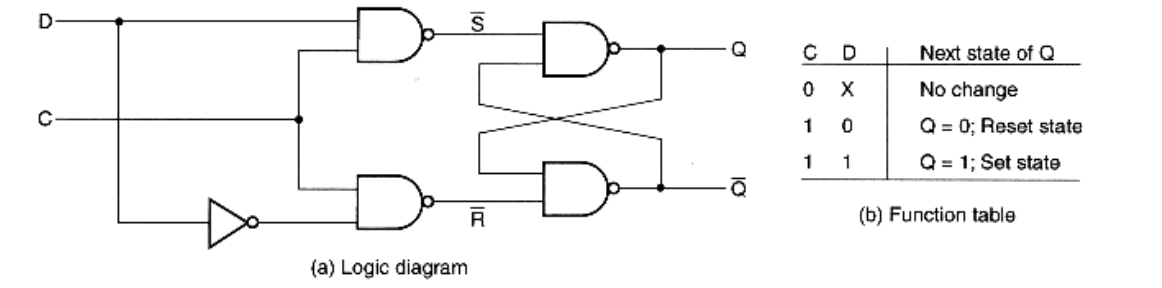
To create an S-R latch, we can wire two NOR gates in such a way that the output of one feeds back to the input of another, and vice versa, like this:



Making S=1 and R=0 “sets” the multivibrator so that Q=1 and not-Q=0. Conversely, making R=1 and S=0 “resets” the multivibrator in the opposite state. When S and R are both equal to 0, the multivibrator’s outputs “latch” in their prior states. When S=R=1 then this is some invalid combination because it does not produce the completed output.

**D-Latch**

The D latch is the simple extension of the gated SR latch which removes the possibility of invalid input states. When the enable line of the D latch is high, the output will always reflect the logic level which is present at the D input. When the input of the D latch falls, the last state of the D latch input is trapped and held in the latch. That is why it is also called as a transparent latch. When enable is asserted, the latch is said to be transparent.

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**Procedure:**

1. Connect the AM2000 trainer to the 220V AC power supply
2. Turn on the trainer and verify the voltage of the power supply using the multimeter. It should be +5V exactly.
3. Install IC74LS02 on the trainer’s board.
4. Wire the circuit according to the diagram by consulting gate IC’s diagram.
5. Use any of the two logic switches from S2 to S9 for inputs S and R respectively.
6. For output indication use any of the LED’s from L0 to L15.
7. Supply the +5v and GND to the pins 14 and 7 of the IC respectively.
8. Test all the possible combinations of inputs and verify the output according to the truth tables of S-R latch.
9. Now install IC IC74LS00 and wire the circuit for D- latch as shown in the above diagram.
10. Make truth table according to the results.

**In case of trouble:**

1. Check the power supply.
2. Check the Vcc and GND at pins 14 and 7 respectively.
3. Check all the wire connections.
4. Check the circuit wiring and remove the breaks.
5. Check the IC using truth table.

**Truth Table for S-R latch [3]**

|  |  |  |  |
| --- | --- | --- | --- |
| **S** | **R** | **Q** |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

**Truth Table for D latch [3]**

|  |  |  |  |
| --- | --- | --- | --- |
| **C** | **D** | **Q** |  |
|  |  |  |  |
|  |  |  |  |
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**Exercise**

**What is the application of S-R latch? [3]**

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**How the invalid situation of S-R latch is compensated in D latch? [3]**

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**Conclusion [3]**

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