** Digital Logic Design**

**Department of Electrical Engineering**

**GC University Lahore**

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| **Lecture Schedule** | Monday (9:30 am – 11:00 am)  Friday (11:00 am – 12:30 pm) | **Semester** | 3rd |
| **Course Code** | EF-2202 | **Credit Hours** | 3 |
| **Instructor** | Engr. Asma Mushtaq | **Pre-requisite** | None |
| **Contact** | asmamushtaq@gcu.edu.pk | **Office** | First Floor  EE Department |
| **Course Description** | The undergraduate course provides the students with a fundamental knowledge about digital logic design. The course starts with the number system. The students are taught how to perform arithmetic in different number systems and perform conversion between different bases. Boolean algebra is introduced. Students are explained how to analyze and design combinational and sequential logic circuits. Counters and shift registers are explained. Hardware descriptor language is introduced. Extensive numerical problems are required in the course to fully comprehend the concepts. At the same time, emphasis is required on the basic concepts so that the students are able to apply their knowledge in different unseen scenarios. The lectures are supplemented by a laboratory. | | |
| **Course Learning Outcomes (CLOs)** | Upon completion of this course, students will be able to:   |  |  |  |  | | --- | --- | --- | --- | | No. | Outcome Statement | Level\* | PLO | | 1 | Learn how to convert numbers between different bases & binary codes and perform arithmetic operations in different systems. | C3 | 1 | | 2 | Perform gate level minimization using Boolean Algebra and K-map and design and analyze combinational logic circuits built from logic gates, decoders, multiplexers and programmable devices. | C3 | 3 | | 3 | Derive equations from truth / state table in order to analyze and design sequential logic circuits including registers, counters, memory and programmable devices. | C3 | 3 |   *\* Bloom’s taxonomy level. C: Cognitive, P: Psychomotor, A: Affective* | | |
| **Weekly Plan** | |  |  |  |  | | --- | --- | --- | --- | | **Week** | **Topics** | **Reading** | **CLO** | | **1-2** | **Number System**   * Number base conversion * Arithmetic in different bases * Complements * Signed binary numbers * Binary codes | Chapter 1 | CLO1 | | **3-4** | **Boolean Algebra and Logic Gates**   * Definition of Boolean algebra * Basic theorems and properties * Boolean functions * Canonical and standard forms * Digital logic gates | Chapter 2 | CLO2 | | **5-6** | **Gate-level minimization**   * K-maps * Product-of-sum (POS) simplification * Don’t care conditions * NAND and NOR implementation * Other simplification methods | Chapter 3 | CLO2 | | **7** | **Design and analysis of combinational logic circuits - I**   * Design and analysis techniques * Binary adder, subtractor, multiplier and magnitude comparator | Chapter 4 | CLO2 | | **8** | **Midterm Examination and Review** | - |  | | **9** | **Design and analysis of combinational logic circuits - II**   * Decoder, encoder, multiplexer and demultiplexer (design, truth table and applications) | Chapter 4 | CLO2 | | **10-12** | **Design and analysis of sequential logic circuits**   * Latches * Flip-flops * Analysis of clocked sequential circuits * State reduction and assignment * Design procedure | Chapter 5 | CLO3 | | **13** | **Registers and Counter**   * Registers * Shift registers * Ripple counters * Synchronous counters | Chapter 6 | CLO3 | | **14-15** | **Memory and programmable logic**   * Memory and its types * Programmable logic devices * FPGA | Chapter 7 | CLO3 | | **16** | **Review** |  |  |   *Note: This lecture plan is based on 3 hours class time per week with a 16 week semester excluding the time for the final examinations* | | |
| **Learning Resources** | **Text Book:**   * M. Morris R. Mano and Michael D. Ciletti , “Digital Design: With an Introduction to the Verilog HDL”, Pearson, 5th Edition, 2012, ISBN-13: 978-0132774208   **Reference Book:**   * M. Morris R. Mano, Charles R. Kime, Tom Martin , “Logic & Computer Design Fundamentals”, Pearson, 5th Edition, 2015, ISBN-13: 978-0133760637 * Ronald Tocci, Neal Widmer, Greg Moss, “Digital Systems”, Pearson, 12th Edition, ISBN-13: 978-0134220130 * Wayne Wolf, “FPGA-Based System Design”, Pearson, 2009, ISBN-13: 978-8131724651 | | |
| **Assessment** | The assessment is done according to the guidelines provided by the University as follows:   |  |  | | --- | --- | | **Assessment Tools** | **Marks** | | Assignments | 10 | | Presentation of Research Paper | 10 | | Quizzes | 10 | | Mid-semester Test | 20 | | Final Exam | 50 |   **Relationship between assessment tools and CLOs:**   |  |  |  |  | | --- | --- | --- | --- | | **Assessment Tools** | **CLO 1** | **CLO 2** | **CLO3** | | Assignments | X | X | X | | Quizzes | X | X | X | | Research Papers Presentation |  |  | X | | Mid-semester Test | X | X |  | | Final Exam |  | X | X |   **Relationship between Program Learning Outcomes (PLOs) and CLOs.**   |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Sr. No.** | **PLOs** | **CLO 1** | **CLO 2** | **CLO 3** | | 1 | Engineering Knowledge | X |  |  | | 2 | Problem Analysis |  | X | X | | 3 | Design / Development of Solutions |  | X | X | | 4 | Investigation |  |  |  | | 5 | Modern Tool Usage |  |  |  | | 6 | The Engineer and Society |  |  |  | | 7 | Environment and Sustainability |  |  |  | | 8 | Ethics |  |  |  | | 9 | Individual and Team-Work |  |  |  | | 10 | Communication |  |  |  | | 11 | Project Management |  |  |  | | 12 | Lifelong Learning |  |  |  | | | |