GCU, Lahore **Roll no. _____**

Electrical Engineering Department **Time:30 minutes**

Digital Logic Design
Assignment 2-CLO2

1. Compare TTL and CMOS logic families in terms of speed, power consumption, noise margin, and fan-out. [5]
2. Simplify the following Boolean expressions to a minimum number of literals: [5]
   a) $ABC + A'B + ABC'$
   b) $(x + y)'(x' + y')'$
   c) $xy + x(wz + wz')$
   d) $(a' + c')(a + b' + c')$
3. Reduce the following Boolean expressions to the indicated number of literals: [5]
   a) $A'C' + ABC + AC'$ to three literals
   b) $(x'y' + z)' + z + xy + wz$ to three literals
   c) $A'B(D' + CD') + B(A + A'CD)$ to one literal
   d) $ABC'D + A'BD + ABCD$ to two literals

4. Given two eight-bit strings *A* = 10110001 and *B* = 10101100, evaluate the eight-bit result after the following logical operations: [5]
   (a)* AND (b) OR (c)* XOR (d)* NOT *A* (e) NOT *B*

5. Draw logic diagrams to implement the following Boolean expressions: [4]
   a) $y = [(u + x')(y' + z)]$
   b) $y = (u \oplus y)' + x$
6. Implement the Boolean function [8]

$$F = xy + x'y' + y'z$$

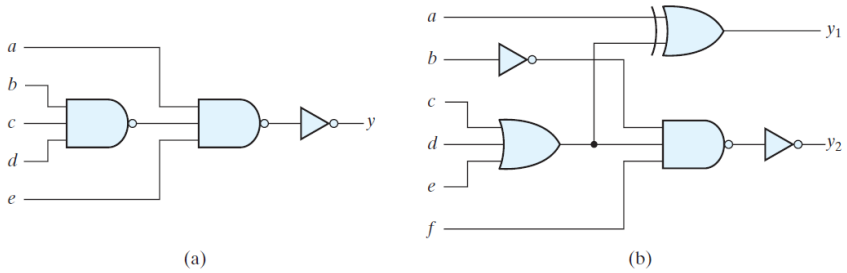
   a) With AND, OR and inverter gates.
   b) With OR and inverter gates
   c) With NAND and inverter gates
   d) With NOR and inverter gates
7. Express the following function as a sum of minterms and as a product of maxterms: [5]

$$F(A, B, C, D) = B'D + A'D + BD$$

8. Convert each of the following expressions into sum of products and product of sums: [5]
   a) $(u + xw)(x + u'v)$
   b) $x' + x(x + y')(y + z')$
9. Show that the dual of the exclusive-OR is equal to its complement. [3]
10. Write Boolean expressions and construct the truth tables describing the outputs of the circuits described by the logic diagrams in Fig (a) and (b). [5]

GCU, Lahore **Roll no. _____**

Electrical Engineering Department **Time:30 minutes**



For the Boolean function [10]

$$F = xy'z + x'y'z + w'xy + wx'y + wxy$$

a) Obtain the truth table of *F*.
b) Draw the logic diagram, using the original Boolean expression.
c) Use Boolean algebra to simplify the function to a minimum number of literals.
d) Obtain the truth table of the function from the simplified expression and show that it is the same as the one in part (a).
e) Draw the logic diagram from the simplified expression, and compare the total number of gates with the diagram of part (b).